CLAIMS

What is claimed is:

1. A method of forming a microwave field effect transistor comprising:

providing a substrate;

providing a heterojunction structure overlying the substrate, wherein the heterojunction structure includes an undoped channel layer with at least one selected from the group consisting of a material layer above, a material layer below, and a material layer above and below the undoped channel layer, the undoped channel layer having a bandgap less than a bandgap of each material layer;

providing a not intentionally doped (NID) layer overlying the heterojunction structure;

providing a heavily doped semiconductor layer overlying the NID layer;

forming a first recess within the heavily doped semiconductor layer, the first recess extending from a source region to a drain region of the microwave field effect transistor;

providing a step gate dielectric overlying the NID layer within the first recess;

providing an interlevel dielectric layer overlying the step gate dielectric;

forming source/drain (S/D) ohmic contacts respectively overlying the source region and the drain region;

forming a top dielectric layer overlying the interlevel dielectric layer and the S/D ohmic contacts;

forming a step gate opening in the top dielectric layer and the interlevel dielectric layer within the first recess between the source region and the drain region;

forming a Schottky gate opening within the step gate opening, the Schottky gate opening extending through the step gate dielectric layer and the NID layer;

providing a barrier metal layer overlying a portion of the heterojunction structure and sidewalls of the NID layer and step gate dielectric within the Schottky gate opening, the barrier metal layer further overlying the step gate dielectric, the NID layer, a portion of the heterojunction structure, and sidewalls of interlevel dielectric and top dielectric within the step gate opening; and

providing a gate metal overlying the barrier metal layer within the Schottky gate opening and within the step gate opening.

2. The method of claim 1, wherein providing the substrate further includes providing a buffer layer overlying the substrate.

3. The method of claim 1, wherein the substrate includes at least one selected from the group consisting of a GaAs, GaN, InP, Si, SiC, and Sapphire.

4. The method of claim 1, wherein the heterojunction structure includes a material system including at least one of GaAs, GaN, and InP.

5. The method of claim 1, wherein each material layer further includes a planar doping layer.

6. The method of claim 5, wherein the planar doping layer includes a Si planar doping layer.

7. The method of claim 1, wherein the undoped channel layer includes at least one selected from the group consisting of GaAs, $In_xGa_{1-x}As$, and $In_xGa_{1-x}N$.

8. The method of claim 1, wherein the NID layer has a thickness on the order of greater than 400 angstroms.

9. The method of claim 8, further wherein the NID layer has a thickness on the order of 400 to 800 angstroms.

10. The method of claim 1, wherein the NID layer includes GaAs.

11. The method of claim 1, wherein the heavily doped semiconductor layer provides a low resistance ohmic contact on the order of approximately $1x10^{-6}$ ohm cm^2.

12. The method of claim 11, wherein the heavily doped semiconductor layer is used for forming source and drain regions of the microwave field effect transistor.

13. The method of claim 1, wherein the step gate dielectric includes a thickness on the order of less than 2,000 angstroms.

14. The method of claim 1, wherein the step gate dielectric includes SiN.

15. The method of claim 1, wherein the interlevel dielectric is for use in forming the gate.

16. The method of claim 15, wherein the interlevel dielectric includes a thickness on the order of 500 to 20,000 angstroms.

17. The method of claim 1, wherein forming the S/D ohmic contacts includes alloying.

18. The method of claim 1, wherein forming the S/D ohmic contacts further includes forming a structure of Ni, Ge , and Au.

19. The method of claim 18, still further including alloying the Ni, Ge, and Au layered structure.

20. The method of claim 1, wherein forming the Schottky gate opening includes at least defining a drain side step gate length.

21. The method of claim 20, wherein the drain side step gate length is on the order of approximately 0.5 to 1.5 micron.

22. The method of claim 20, wherein a portion of the step gate dielectric layer separates the step gate from an underlying portion of the NID layer on a drain side by at least the drain side step gate length.

23. The method of claim 1, wherein the barrier metal layer provides at least one selected from the group consisting of an adhesion layer, and maintaining a Schottky contact at elevated temperatures of the microwave field effect transistor.

24. The method of claim 1, wherein the barrier metal layer includes a refractory metal.

25. The method of claim 1, wherein the barrier metal layer includes one selected from the group consisting of WSi, TiWN, TiPt and TiPd.

26. The method of claim 1, wherein the barrier metal layer further includes overlying a portion of the top dielectric layer and the interlevel dielectric outside of the step gate opening.

27. The method of claim 1, wherein the gate metal includes a low resistivity gate metal.

28. The method of claim 1, wherein the gate metal includes at least one selected from the group consisting of gold, copper, aluminum, and silver.

29. A method of forming a microwave field effect transistor comprising:

providing a substrate;

providing a heterojunction structure overlying the substrate, wherein the heterojunction structure includes an undoped channel layer with a material layer above and below the undoped channel layer, the undoped channel layer having a bandgap less than a bandgap of each material layer

and each material layer including a planar doping layer, further wherein the heterojunction structure includes a material system including at least one of GaAs, GaN, and InP;

providing a not intentionally doped (NID) layer overlying the heterojunction structure;

providing a heavily doped semiconductor layer overlying the NID layer;

forming a first recess within the heavily doped semiconductor layer, the first recess extending from a source region to a drain region of the microwave field effect transistor;

providing a step gate dielectric overlying the NID layer within the first recess;

providing an interlevel dielectric layer overlying the step gate dielectric;

forming source/drain (S/D) ohmic contacts overlying respective source and drain regions;

forming a top dielectric layer overlying the interlevel dielectric layer and the S/D ohmic contacts;

forming a step gate opening in the top dielectric layer and the interlevel dielectric layer within the first recess between the source and drain regions;

forming a Schottky gate opening within the step gate opening, the Schottky gate opening extending through the step gate dielectric layer and the NID layer;

providing a barrier metal layer overlying a portion of the heterojunction structure and sidewalls of the NID layer and step gate dielectric within the Schottky gate opening, the barrier metal layer further overlying the step gate dielectric, the NID layer, a portion of the

heterojunction structure, and sidewalls of interlevel dielectric and top dielectric within the step gate opening; and

providing a gate metal overlying the barrier metal layer within the Schottky gate opening and within the step gate opening.

30. The method of claim 29, wherein the NID layer includes a GaAs layer having a thickness on the order of 400 to 800 angstroms.

31. A microwave field effect transistor comprising:

a heterojunction structure overlying a substrate, wherein the heterojunction structure includes an undoped channel layer with at least one selected from the group consisting of a material layer above, a material layer below, and a material layer above and below the undoped channel layer, the undoped channel layer having a bandgap less than a bandgap of each material layer;

a not intentionally doped (NID) layer overlying a portion of the heterojunction structure;

a heavily doped semiconductor source region overlying a portion of the NID layer;

a heavily doped semiconductor drain region overlying another portion of the NID layer and spaced from the source region by a first region;

a step gate dielectric overlying a portion of the NID layer within the first region;

an interlevel dielectric overlying a portion of the step gate dielectric;

source/drain (S/D) ohmic contacts overlying portions of respective source and drain regions;

a top dielectric layer overlying a portion of the interlevel dielectric layer and the S/D ohmic contacts, wherein the top dielectric layer and the

interlevel dielectric layer further include a step gate region within the first region between the source and drain regions, further wherein a Schottky gate region is disposed within the step gate region, the Schottky gate region extending through the step gate dielectric layer and the NID layer;

a barrier metal layer overlying a portion of the heterojunction structure and sidewalls of the NID layer and step gate dielectric within the Schottky gate region, the barrier metal layer further overlying the step gate dielectric, the NID layer, a portion of the heterojunction structure, and sidewalls of interlevel dielectric and top dielectric within the step gate region; and

a gate metal overlying the barrier metal layer within the Schottky gate region and within the step gate region.

32. The microwave field effect transistor of claim 31, wherein the NID layer has a thickness on an order of greater than 400 angstroms.

33. The microwave field effect transistor of claim 32, further wherein the NID layer has a thickness on an order of 400 to 800 angstroms.